ABSTRACT

A method of fabricating an integrated circuit on a wafer includes forming a gate electrode stack over a gate dielectric and forming nitride spacers along sidewalls of the gate electrode stack other than along lowermost portions of the sidewalls. Subsequently, a reoxidation process is performed with respect to the gate dielectric. By providing the nitride spacers along exposed surfaces of conductive barrier and metal layers of the word line stack, those surfaces can be passivated, thereby preventing or reducing the conversion of those layers to non-conductive compounds during the reoxidation process. At the same time, the nitride spacers can be formed so that they do not interfere with the subsequent reoxidation of the gate dielectric. An integrated circuit having a gate electrode stack with nitride spacers extending along sidewalls of the gate electrode stack other than along lowermost portions of the sidewalls is also disclosed.

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